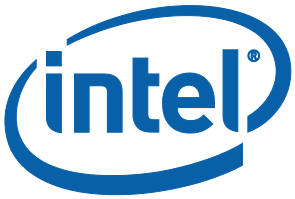

Intel® Atom™ Processor Z6xx Series

Datasheet

For the Intel® Atom™ Processor Z670 on 45-nm Process Technology

April 2011

Revision 001

Document Number: 325310-001

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Revision History

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325314	001	• Initial release.	April 2011

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1 Introduction

The datasheet describes the architecture, features, buffers, signal descriptions, power management, pin states, operating parameters, and specifications for the Intel® Atom™ Processor Z670 (Core Processor and North Complex).

Intel® Atom™ Processor Z670 is the next generation low power IA-32 processor that is based on the new re-partitioning architecture targeted for tablets and sleek netbooks. The main components of Intel® Atom™ Processor Z670 are: an IA-compatible processor core derived from the Intel® Atom™ processor, a single-channel 32-bit DDR2 memory controller, a 3-D graphics engine, video decode engines, a 2-D display controller, a cDMI interface link to the Intel® SM35 Express Chipset, and an LVDS interface to support a primary display interface link. An additional cDVO interface is used for pixel data to the Intel® SM35 Express Chipset.

Throughout this document, the Intel® Atom™ Processor Z670 is referred as the processor and Intel® SM35 Express Chipset is referred to as the chipset.

1.1 Processor Features

The following list provides some of the key features on this processor:

- Supports Intel® Hyper-Threading Technology
- 2-wide instruction decode and in-order execution
- 512 KB, 8 way L2 cache
- Support for IA 32-bit architecture
- FCMB3 packaging technology
- Thermal management support using TM1 and TM2
- On die Digital Thermal Sensor (DTS) for thermal management support using Intel® Thermal Monitor 1 (TM1) and Intel® Thermal Monitor 2 (TM2)
- Advanced power management features including Enhanced Intel® SpeedStep® Technology
- Supports C0/C1(e)/C2(e)/C4(e) power states
- Intel Deep Power Down Technology (C6)

1.2 Interfaces

1.2.1 System Memory Support

- One channel of DDR2 memory
- 32-bit data bus
- Memory DDR2 transfer rates of 800 MT/s
- Supports 1 Gb, and 2 Gb devices
- Supports total memory size of 1 GB, and 2 GB
- Provides aggressive power management to reduce power consumption when idle
- Provides proactive page closing policies to close unused pages

1.2.2 Display Controller

- Seven display planes: Display Plane A, Display Plane B, Display C/sprite, Overlay, Cursor A, Cursor B, and VGA
- Display Pipe A: Supports LVDS display interface
- Display Pipe B: Supports HDMI via chipset
- Maximum resolution (LVDS display):
  - 1366 x 768 @ 18 bpp and 60 fps
- Supports 18 bpp
- Supports Non-Power of 2 Tiling
- Output pixel width: 24-bit RGB
- Supports NV12 video data format
- Supports 3 x 3 panel fitter
- Dynamic Power Saving Technology (DPST) 3.0
- Support 16 x 256 byte tile size
- Supports overlay
- Supports global constant alpha blending

1.2.3 cDMI

- Peak raw BW of cDMI link per direction = 400 MT/s using a quad-pumped 8-bit transmit and an 8-bit receive data bus
- Supports low power management schemes
- Supports CMOS interface

1.2.4 cDVO

- Peak raw BW of 800MT/s
- Supports low power management schemes
- Supports AGTL+ interface

1.2.5 LVDS

- Maximum resolution (internal display) of:
- 1366 x 768 @ 18 bpp and 60 fps
- Dot clock range from 20–83 MHz
- Four differential signal pairs: Three data pairs (up to 581 Mbps on each data link) and one clock pair
- Supports 18 bpp packed and 18 bpp loosely packed pixel formats
- Supports 24 bpp with a limited number of validated panels.

1.3 Terminology

Acronym	Description
ACPI	Advanced Configuration and Power Interface
AGTL+	Assisted Gunning Transceiver Logic Plus
CKE	Clock enable
CMOS	Complementary metal-oxide semiconductor
cDMI	CMOS Direct Media Interface
cDVO	CMOS Digital Video Output
DDR2	Second-generation Double Data Rate SDRAM memory technology
DQ	Memory data
DQS	Memory data strobe
DTS	Digital thermal sensor
FSB	Front side bus
GPIO	General purpose input/output
GTL	Gunning Transceiver Logic
HPLL	Host phase lock loop
IERR	Internal error
iFSB	Internal front side bus
LFM	Low Frequency Mode
LGI	Legacy interface

Acronym	Description
LVDS	Low Voltage Differential Signaling, a high speed, low power data transmission standard used for display connections to LCD panels
MSR	Model-specific register
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved, so the loss of solder joint continuity at end of life conditions will not affect the overall product functionality.
NMI	Non-maskable interrupt
North Complex	Processor unicore which processor memory controller, Power Management Unit and internal FSB Logic
ODT	On Die Termination
PCH	Platform Controller Hub
PMIC	Power Management Integrated Circuit
PMU	Power Management Unit
RCOMP	Resistor compensation
SCK	System clock
SR	Self-Refresh
TAP	Test access point
TCC	Thermal control circuit
TDP	Thermal Design Power
TM1	Thermal Monitor 1
TM2	Thermal Monitor 2
VR	Voltage regulator

1.4 Reference Documents

Document	Location / Comments
Intel® Atom™ Processor Z6xx Series Specification Update For the Intel® Atom™ Processor Z670 on 45-nm Process Technology	325309-001
Intel® SM35 Express Chipset Datasheet	325308-001
Intel® SM35 Express Chipset Specification Update	325307-001
AP-485, Intel® Processor Identification and the CPUID Instruction	http://www.intel.com/Assets/PDF/appnote/241618.pdf

Document	Location / Comments
Intel® 64 and IA-32 Architectures Software Developer's Manuals	
Volume 1: Basic Architecture	http://www.intel.com/products/processor/manuals/index.htm
Volume 2A: Instruction Set Reference, A-M	
Volume 2B: Instruction Set Reference, N-Z	
Volume 3A: System Programming Guide	
Volume 3B: System Programming Guide	

NOTES:

1. Contact your Intel representative for the latest revision and document number of this document.

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2 Signal Descriptions

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type.

Table 2-1. Signal Types

Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

Table 2-2. Buffer Types

Buffer Type	Interface	Description
AGTL+	cDVO, cDMI	**Assisted Gunning Transceiver Logic Plus:** CMOS open drain interface signals that require termination. Refer to the AGTL+ I/O Specification for complete details.
CMOS, CMOS_OD	cDMI, cDVO, LGI, LGIE	**1.05-V CMOS buffer** or **CMOS open drain**.
Analog	All	**Analog reference or output:** This may be used as a threshold voltage or for buffer compensation.
LVDS	LVDS	**Low-voltage differential signal output buffers**
CMOS1.8	DDR2	**1.8-V CMOS buffer:** These buffers can be configured as Stub Series Termination Logic.

2.1 Signal Description

This section provides a detailed description of Processor signals. The signals are arranged in functional groups according to their associated interface.

2.1.1 System Memory Interface

Table 2-3. System Memory Interface Signals

Signal	Direction Type	Description
SM_CK0	O CMOS1.8	**Differential DDR clock**
SM_CK0#	O CMOS1.8	**Complementary differential DDR clock.**

Signal	Direction Type	Description
SM_SREN#	I CMOS1.8	**Self-refresh enable:** Signal from the chipset asserted after processor places DDR in self-refresh.
SM_CKE[1:0]	O CMOS1.8	**Clock enable:** SM_CKE is used for power control of the DRAM devices. There is one SM_CKE per rank.
SM_CS[1:0]#	O CMOS1.8	**Chip select:** These signals determine whether a command is valid in a given cycle for the devices connected to it. There is one chip select signal for each rank.
SM_RAS#	O CMOS1.8	**Row address strobe:** This signal is used with SM_CAS# and SM_WE# (along with SM_CS#) to define commands.
SM_CAS#	O CMOS1.8	**Column address strobe:** This signal is used with SM_WE#, SM_RAS#, and SM_CS# to define commands.
SM_WE#	O CMOS1.8	**Write enable:** This signal is used with SM_CAS#, SM_RAS#, and SM_CS# to define commands.
SM_ODT[1:0]	O CMOS1.8	**On Die Termination:** Active Termination Control.
SM_BS[2:0]	O CMOS1.8	**Bank select:** These signals define which banks are being addressed within each Rank.
SM_MA[14:0]	O CMOS1.8	**Multiplexed address:** SM_MA signals provide multiplexed row and column address to memory.
SM_DQ[31:0]	I/O CMOS1.8	**Data lines:** SM_DQ signals interface to the DRAM data bus.
SM_DQS[3:0]	I/O CMOS1.8	**Data strobes:** These signals are used during writes and are centered with respect to data. During reads, these signals are driven by memory devices and are edge aligned with data.
SM_DM[3:0]	O CMOS1.8	**Data mask:** One bit per byte indicating which bytes should be written.
SM_RCVENIN	I CMOS1.8	**Receive enable in:** This input enables the SM_DQS input buffers during reads.
SM_RCVENOUT	O CMOS1.8	**Receive enable out:** Part of the feedback used to enable the DQS input buffers during reads.
SM_RCOMP	I Analog	**RCOMP:** Connected to high-precision resistor on the motherboard. Used to dynamically calibrate the driver strengths.

2.1.2 cDMI Interface

Table 2-4. cDMI Interface Signal

Signal	Direction Type	Description
CDMI_RCOMP[1:0]	I Analog	**CDMI_RCOMP:** Connected to high-precision resistors on the motherboard. Used for compensating cDMI pull-up/pull-down impedances.
CDMI_TX[7:0]	O CMOS	**Data output:** quad-pump (strobed) data bus from Processor to PCH.
CDMI_TXCHAR#	O CMOS	**Data control character data control character output:** Quad-Pump (strobed) indication that CDMI_TX[7:0] contains a control character instead of data.
CDMI_TXDPWR#	O CMOS	**Line wakeup for output:** When asserted, the PCH will power-up its receivers on CDMI_TX[7:0] and CDMI_TXCHAR#, and CDMI_TXSTB[0].
CDMI_TXSTB_ODD#, CDMI_TXSTB_EVEN#	O CMOS	**Data strobe output:** Strobes for CDMI_TX[7:0] and CDMI_TXCHAR#.
CDMI_RX[7:0]	I CMOS	**Data input:** Quad-Pump (strobed) data bus from PCH to Intel® Atom™ Processor Z670.
CDMI_RXCHAR#	I CMOS	**Data control character input:** Quad-pump (strobed) indication that CDMI_RX[7:0] contains a control character instead of data.
CDMI_RXDPWR#	I CMOS	**Line wakeup for input:** Power enable from PCH. Used to enable Receivers on CDMI_RX[7:0], CDMI_RXCHAR#, and CDMI_RXSTB_ODD#.
CDMI_RXSTB_ODD#, CDMI_RXSTB_EVEN#	I CMOS	**Data strobe input:** Strobes for CDMI_RX[7:0] and CDMI_RXCHAR#.
CDMI_GVREF	I Analog	**Strobe Signals' Reference Voltage for DMI:** Externally set by means of a passive voltage divider. Voltage should be 1/2 VCCP when configured for CMOS.
CDMI_CVREF	I Analog	**Non-Strobe Signals' Reference Voltage for DMI:** Externally set by means of a passive voltage divider. Voltage should be 1/2 VCCP when configured for CMOS.

2.1.3 cDVO Interface

Table 2-5. cDVO Interface Signals

Signal	Direction Type	Description
CDVO_RCOMP[1:0]	I Analog	**CDVO_RCOMP:** Connected to high-precision resistors on the motherboard. Used for compensating pull-up/pull-down impedances.
CDVO_TX[5:0]	O AGTL+	**Data output:** Quad-pump (strobed) data bus from Intel® Atom™ Processor Z670 to PCH.

Signal	Direction Type	Description
CDVO_STALL#	I AGTL+	**Stall:** Allows PCH to throttle the sending of display data.
CDVO_TXDPWR#	O AGTL+	**Line wakeup for output:** When asserted, the PCH will power-up its receivers on CDVO_TX[5:0] and CDVO_TXSTB_ODD#.
CDVO_TXSTB_ODD#, CDVO_TXSTB_EVEN#	O AGTL+	**Data strobe output:** Strobes for CDVO_TX[5:0].
CDVO_VBLANK#	I AGTL+	**Vertical blank:** Indication from PCH indicating the start of the vertical blank period.
CDVO_GVREF	I Analog	**Strobe signals' reference voltage for CDVO:** Externally set by means of a passive voltage divider. Voltage should be 2/3 V_{CCP} when configured for GTL.
CDVO_CVREF	I Analog	**Non-Strobe Signals' Reference Voltage for CDVO:** Externally set by means of a passive voltage divider. Voltage should be 2/3 V_{CCP} when configured for GTL.

2.1.4 LVDS Display Port Interface

Table 2-6. LVDS Display Port Interface Signals

Signal	Direction Type	Description
LA_DATAN[3:0]	O LVDS	**Differential Data Output (Negative)**
LA_DATAP[3:0]	O LVDS	**Differential Data Output (Positive)**
LA_CLKN	O LVDS	**Differential Clock Output (Negative)**
LA_CLKP	O LVDS	**Differential Clock Output (Positive)**
LA_IBG	I Analog	**External Voltage Ref BG:** Connected to high-precision resistor on motherboard to VSS.
LA_VBG	I Analog	**External Voltage Ref BG:** Requires external 1.25 V ±2% supply.

2.1.5 LGI/LGIe (Legacy) Signals

Table 2-7. LGI/LGIe Legacy Signals

Signal	Direction Type	Description
VID[6:0]	O CMOS	**Voltage ID:** Connects to PMIC. Indicates a desired voltage for either V_{CC} or V_{NN} depending on the VIDEN[] pins. Resolution of 12.5 mV.
VIDEN[1:0]	O CMOS	**Voltage ID enable:** Connects to PMIC. Indicates which voltage is being specified on the VID pins: 00 = VID is invalid 01 = VID = V_{CC} 10 = VID = V_{NN} 11 = RSVD
THERMTRIP#	O CMOS_OD	**Catastrophic Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 120° C. This condition is signaled to the system by the THERMTRIP# (Thermal Trip) pin.
PROCHOT#	I/O O: CMOS_OD I: CMOS	**Processor hot:** As an output, PROCHOT# (processor hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#.
VSSSENSE, VCCSENSE, VNNSENSE	O Analog	**Voltage sense:** Connects to PMIC. Voltage Regulator must connect feedback lines for V_{CC}, V_{SS}, and V_{NN} to these pins on the package.
BSEL1	O CMOS	**BSEL1:** Selects external reference clock for DDR2, cDMI, and cDVO frequencies. 1 = Reserved 0 = 100 MHz, for cDVO/DDR2-800MT/s.
IERR	O CMOS	**IERR:** Internal error indication (debug). Positively asserted. Asserted when the processor has had an internal error and may have unexpectedly stopped executing. Assertion of IERR is usually accompanied by a SHUTDOWN transaction internal to Processor which may result in assertion of NMI to the processor. The processor will keep IERR asserted until the POWERMODE[] pins take Processor to reset or Processor receives a reset message over cDMI.
GTLREF0	I Analog	**Voltage reference for BPM[3:0]#:** 2/3 V_{CCP} by means of an external voltage divider: 1k Ω to V_{CCP}, 2 KΩ to V_{SS}.
GTLREF1	I Analog	**Voltage reference:** 2/3 V_{CCP} by means of external voltage divider: 1 KΩ to V_{CCP}, 2 KΩ to V_{SS}.

Signal	Direction Type	Description
PWRMODE[2:0]	I CMOS	**Power mode:** The chipset is expected to sequence Processor through various states using the POWERMODE[] pins to facilitate cold reset, and warm reset.
BCLK_P/N	I CMOS	**Reference clock:** Differential 100 MHz.

2.1.6 Debug and Miscellaneous Signals

Table 2-8. Debug and Miscellaneous Signals

Signal	Direction Type	Description
BPM[3:0]#	I/O AGTL+	**Break/perf monitor:** Various debug input and output functions.
PRDY#	I/O AGTL+	**Probe mode ready:** The processor's response to a PRDY# assertion. This signal indicates that the processor is in probe mode. Input is unused.
PREQ#	I/O AGTL+	**Probe mode request:** Assertion is a request for the processor to enter probe mode. Processor will respond with PRDY# assertion once it has entered. PREQ# can be enabled to cause the processor to break from C4 and C6. Internal 51 Ω pull up, so no external pull-up required.
TCK	I CMOS	**Processor JTAG test clock:** This signal provides the clock input for the processor Test Bus (also known as the Test Access Port). Requires an external 51 Ω resistor to Vss.
TDI	I CMOS	**Processor JTAG test data input:** This signal transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support. Requires an external 51 Ω resistor to V_{CCP}.
TDO	O OD	**Processor JTAG test data output:** This signal transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support. Requires an external 51 Ω resistor to V_{CCP}.
TMS	I CMOS	**Processor JTAG test mode select:** A JTAG specification support signal used by debug tools. Requires an external 51 Ω resistor to V_{CCP}.
TRST#	I CMOS	**Processor JTAG test reset:** Asynchronously resets the Test Access Port (TAP) logic. TRST# must be driven asserted (low) during processor power on reset. Processor has an internal 51 Ω pull-up to V_{CCP}, unlike the Pentium M processor, the Intel® Core™2 processor, and the Intel® Atom™ Z5xx processor. The Processor pull-up matches the Intel® Pentium® 4 processor and the IEEE specification.
RSVD		These pins should be treated as no connection (NC).

2.1.7 Power Signals

Table 2-9. Power Signals

Signal	Type	Description
V_{CC}	PWR	**Processor core supply voltage:** Power supply is required for processor cycles.
V_{NN}	PWR	**North Complex logic and graphics supply voltage.**
V_{CCP}	PWR	**cDMI, cDVO, LGI, LGIe, JTAG, RCOMP, and power gating supply voltage.** Needed for most bus accesses. Cannot be connected to $V_{CCPAOAC}$ during Standby or Self-Refresh states.
V_{CCPDDR}	PWR	**DDR DLL and logic supply voltage:** Required for memory bus accesses. Requires a separate rail with noise isolation.
$V_{CCPAOAC}$	PWR	**JTAG, C6 SRAM supply voltage:** Needs to be on in Active or Standby.
LVD_VBG	PWR	**LVDS band gap supply voltage:** Needed for LVDS display.
V_{CCA}	PWR	**HPLL Analog PLL and thermal sensor supply voltage.**
V_{CCA180}	PWR	**LVDS analog supply voltage:** Needed for LVDS display. Requires a separate rail with noise isolation.
V_{CCD180}	PWR	**LVDS I/O supply voltage:** Needed for LVDS display.
$V_{CC180SR}$	PWR	**DDR2 self-refresh supply voltage:** Powered during Active, Standby, and Self-Refresh states.
V_{CC180}	PWR	**DDR2 I/O supply voltage** Required for memory bus accesses. Cannot be connected to $V_{CC180SR}$ during Standby or Self-Refresh states.
V_{MM}	PWR	**I/O supply voltage.**
V_{SS}		**Ground pin**

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3 Power Management

Processor supports fine grain power management by having several partitions of voltage islands created through on-die power switches. The Intel® Smart Power Technology (Intel® SPT) software determines the most power efficient state for the platform at any given point in time and then provides guidance to turn ON or OFF different voltage islands on processor. For the scenario where Intel® SPT has directed the processor to go into an Intel® SIT idle mode, the processor waits for all partitions with shared voltage to reach a safe point and then turns them off.

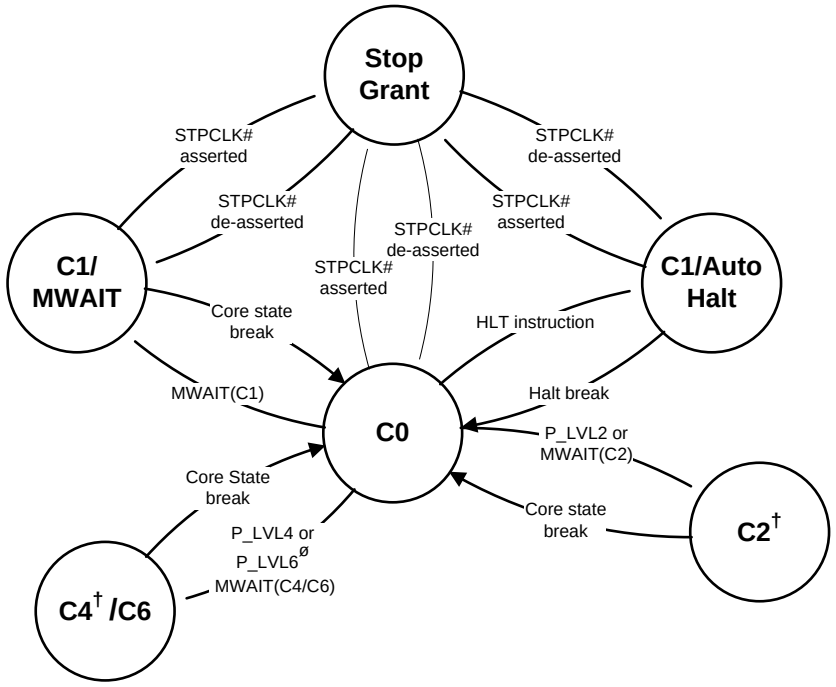
3.1 Processor Core Low Power Features

When the processor core is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies.

Figure 3-1 shows the thread low power states. Figure 3-2 shows the package low power states.

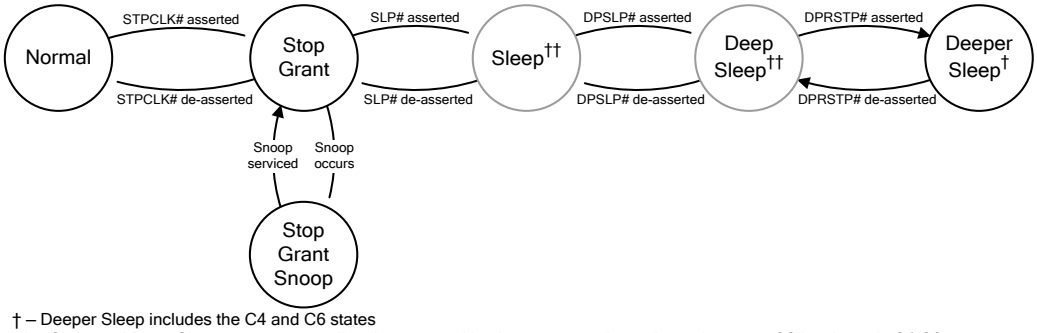
Note: STPCLK#, DPSLP#, and DPRSTP are internal signals only.

Figure 3-1. Thread Low Power States



halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event) AND STPCLK# high (not asserted)
† — STPCLK# assertion and de-assertion have no effect if a core is in C2 or C4.
Ø — P_LVL6 read is issued once the L2 cache is reduced to zero.

Figure 3-2. Package Low Power States



† – Deeper Sleep includes the C4 and C6 states
†† – Sleep and Deep Sleep are not states directly supported by the processor, but rather sub-states of Silverthorne's C4/C6

3.1.1 Cx State Definitions

- **C0 State—Full On**

  This is the only state that runs software. All clocks are running and the processor core is active. The processor can service snoops and maintain cache coherency in this state. All power management for interfaces, clock gating, are controlled at the unit level.

- **C1 State—Auto-Halt**

  The first level of power reduction occurs when the core processor executes an Auto-Halt instruction. This stops the execution of the instruction stream and greatly reduces the core processor's power consumption. The core processor can service snoops and maintain cache coherency in this state. The Processor North Complex logic does not distinguish C1 from C0 explicitly.

- **C2 State—Stop Grant**

  The next level of power reduction occurs when the core processor is placed into the Stop Grant state. The core processor can service snoops and maintain cache coherency in this state. The North Complex only supports receiving a single Stop Grant.

  Entry into the C2 state will occur after the core processor requests C2 (or deeper). C2 state will be exited, entering the C0 state, when a break event is detected. Processor must ensure that the DLLs are awake and the memory will be out of self-refresh at this point.

- **C1E and C2E States**

  C1E and C2E states are transparent to the north complex logic. The C1E state is the same as the C1 state, in that the core processor emits a HALT cycle when entering the state. There are no other visible actions from the core processor.

  The C2E state is the same as the C2 state, in that the core processor emits a Stop Grant cycle when entering the state. There are no other visible actions from the core processor.

- **C4 State—Deeper Sleep**

  In this state, the core processor shuts down its PLL and cannot handle snoop requests. The core processor voltage regulator is also told to reduce the processor's voltage. During the C4 state, the North Complex will continue to handle traffic to memory so long as this traffic does not require a snoop (i.e., no coherent traffic requests are serviced).

  The C4 state is entered by receiving a C4 request from the core processor/OS. The exit from C4 occurs when the North Complex detects a snoopable event or a break event, which would cause it to wake up the core processor and initiate the C0 sequence.

- **C4E**

  The C4E state is essentially the same as the C4 state except that the core processor will transition to the Low Frequency Mode (LFM) frequency and voltage upon entry and exit of this state.

- **C6—Deep Power Down**

  Prior to entering the C6 state, the core processor will flush its cache and save its core context to a special on-die SRAM on a different power plane. Once the C6 entry sequence has completed, the core processor's voltage can be completely shut off.

  The key difference for the North Complex logic between the C4 state and the C6 state is that since the core processor's cache is empty, there is no need to perform snoops on the internal FSB. This means that bus master events (which would cause a popup from the C4 state to the C2 state) can be allowed to flow unimpeded during the C6 state. However, the core processor must still be returned to the C0 state to service interrupts.

  A residency counter is read by the core processor to enable an intelligent promotion/demotion based on energy awareness of transitions and history of residencies/transitions.

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4 Electrical Specifications

This chapter contains signal group descriptions, absolute maximum ratings, voltage identification and power sequencing. This chapter also includes DC specifications.

4.1 Power and Ground Balls

The processor has Vcc and Vss (ground) inputs for on-chip power distribution. All power balls must be connected to their respective processor power planes, while all Vss balls must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The Vcc balls must be supplied with the voltage determined by the processor Voltage Identification (VID) signals.

4.2 Decoupling Guidelines

Due to large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values, if bulk decoupling is not adequate. Larger bulk storage (C_{BULK}), such as electrolytic capacitors, supply current during longer lasting changes in current demand (for example, coming out of an idle condition). Similarly, capacitors act as a storage well for current when entering an idle condition from a running condition. To keep voltages within specification, output decoupling must be properly designed.

Caution: Design the board to ensure that the voltage provided to the processor remains within the specification. Failure to do so can result in timing violations or reduced lifetime of the processor.

4.3 Voltage Rail Decoupling

The voltage regulator solution needs to provide:

- Bulk capacitance with low effective series resistance (ESR).
- A low path impedance from the regulator to the processor.
- Bulk decoupling to compensate for large current swings generated during power-on, or low-power idle state entry/exit.

The power delivery solution must ensure that the voltage and current specifications are met, as defined in Table 4-4.

4.4 Voltage Identification (VID)

The V_{CC} and V_{NN} voltage inputs use two encoding pins (VIDEN[1:0]) to enable the VID pin inputs and seven voltage identification pins (VID[6:0]) to select the power supply voltage. The VID/VIDEN pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 4-2 specifies the voltage level corresponding to the state of VID[6:0]. A “1” in this refers to a high-voltage level and a “0” refers to a low-voltage level. For more details about PMIC design to support the processor power supply requirements, refer to the vendor’s specification.

4.4.1 VID Enable

Both V_{CC} and V_{NN} are variable in Intel® Atom™ Processor Z670. Processor implements a new VID mechanism that minimizes the number of required pins. The VID for V_{NN} and V_{CC} are multiplexed on to the same set of pins and a separate 2-bit enable/ID is defined to specify what the driven VID corresponds to. One of the combinations is used to notify that the VID is invalid. This is used when the processor is in C6/Standby to tri-state the VID pins to save power.

Table 4-1. VIDEN Encoding

VIDEN[1:0]	Description
00b	VID is invalid
01b	VID for V_{CC}
10b	VID for V_{NN}
11b	Reserved

4.4.2 VID Table

Note:

1. Processor will not support the entire range of the voltages listed in the VID table (grayed out).
2. VID codes below 0.3 V are not supported for V_{CC}.

Table 4-2. VID Table

VID[6:0]	V_{CC} / V_{NN}	VID[6:0]	V_{CC} / V_{NN}	VID[6:0]	V_{CC} / V_{NN}	VID[6:0]	V_{CC} / V_{NN}
00h	1.5000V	20h	1.1000V	40h	0.7000V	60h	0.3000V
01h	1.4875V	21h	1.0875V	41h	0.6875V	61h	0.2875V
02h	1.4750V	22h	1.0750V	42h	0.6750V	62h	0.2750V
03h	1.4625V	23h	1.0625V	43h	0.6625V	63h	0.2625V
04h	1.4500V	24h	1.0500V	44h	0.6500V	64h	0.2500V
05h	1.4375V	25h	1.0375V	45h	0.6375V	65h	0.2375V
06h	1.4250V	26h	1.0250V	46h	0.6250V	66h	0.2250V
07h	1.4125V	27h	1.0125V	47h	0.6125V	67h	0.2125V
08h	1.4000V	28h	1.0000V	48h	0.6000V	68h	0.2000V
09h	1.3875V	29h	0.9875V	49h	0.5875V	69h	0.1875V
0Ah	1.3750V	2Ah	0.9750V	4Ah	0.5750V	6Ah	0.1750V
0Bh	1.3625V	2Bh	0.9625V	4Bh	0.5625V	6Bh	0.1625V
0Ch	1.3500V	2Ch	0.9500V	4Ch	0.5500V	6Ch	0.1500V
0Dh	1.3375V	2Dh	0.9375V	4Dh	0.5375V	6Dh	0.1375V
0Eh	1.3250V	2Eh	0.9250V	4Eh	0.5250V	6Eh	0.1250V
0Fh	1.3125V	2Fh	0.9125V	4Fh	0.5125V	6Fh	0.1125V
10h	1.3000V	30h	0.9000V	50h	0.5000V	70h	0.1000V
11h	1.2875V	31h	0.8875V	51h	0.4875V	71h	0.0875V
12h	1.2750V	32h	0.8750V	52h	0.4750V	72h	0.0750V
13h	1.2625V	33h	0.8625V	53h	0.4625V	73h	0.0625V
14h	1.2500V	34h	0.8500V	54h	0.4500V	74h	0.0500V
15h	1.2375V	35h	0.8375V	55h	0.4375V	75h	0.0375V
16h	1.2250V	36h	0.8250V	56h	0.4250V	76h	0.0250V
17h	1.2125V	37h	0.8125V	57h	0.4125V	77h	0.0125V
18h	1.2000V	38h	0.8000V	58h	0.4000V	78h	0.0000V
19h	1.1875V	39h	0.7875V	59h	0.3875V	79h	0.0000V
1Ah	1.1750V	3Ah	0.7750V	5Ah	0.3750V	7Ah	0.0000V
1Bh	1.1625V	3Bh	0.7625V	5Bh	0.3625V	7Bh	0.0000V

VID[6:0]	V_{CC} / V_{NN}	VID[6:0]	V_{CC} / V_{NN}	VID[6:0]	V_{CC} / V_{NN}	VID[6:0]	V_{CC} / V_{NN}
1Ch	1.1500V	3Ch	0.7500V	5Ch	0.3500V	7Ch	0.0000V
1Dh	1.1375V	3Dh	0.7375V	5Dh	0.3375V	7Dh	0.0000V
1Eh	1.1250V	3Eh	0.7250V	5Eh	0.3250V	7Eh	0.0000V
1Fh	1.1125V	3Fh	0.7125V	5Fh	0.3125V	7Fh	0.0000V

4.5 Absolute Maximum Ratings

Table 4-3 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, then when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 4-3. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Note
V_{CC}	Processor core supply voltage	-0.3	1.1	V	
V_{NN}	North Complex logic and GFX supply voltage	-0.3	0.95	V	
V_{CCP}/V_{CCQ}	cDMI, cDVO, LGI, LGIe	-0.3	1.1	V	
V_{CCPDDR}	1.05-V DDR2 DLL and logic supply voltage	-0.3	1.1	V	
$V_{CCPAOAC}$	1.05-V JTAG, C6 SRAM	-0.3	1.1	V	
V_{MM}	1.2-V I/O supply voltage	-0.3	1.25	V	
LVD_VBG	1.25-V LVDS band gap supply voltage	-0.1	1.28	V	
V_{CCA}	1.5-V HPLL analog PLL and thermal sensor supply voltage	-0.3	1.575	V	
V_{CCA180}	1.8-V LVDS analog supply voltage	-0.3	1.9	V	

Symbol	Parameter	Minimum	Maximum	Unit	Note
V_{CCD180}	1.8-V LVDS I/O supply voltage	-0.3	1.9	V	
$V_{CC180SR}$	1.8-V DDR2 self-refresh supply voltage	-0.4	1.9	V	
V_{CC180}	1.8-V DDR2 I/O supply voltage	-0.4	1.9	V	
T_J	Operational junction temperature	0	90	°C	1,2
$T_{SUSTAINED\ STORAGE}$	The ambient storage temperature limit (in shipping media) for a sustained period of time.	-5 °C	40 °C	°C	4
$RH_{SUSTAINED\ STORAGE}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24 °C			4,5
$TIME_{SUSTAINED\ STORAGE}$	A prolonged or extended period of time; typically associated with customer shelf life.	0	6	Months	5

NOTE:

1. As measured by the activation of the on-die Intel® Thermal Monitor. The Intel Thermal Monitor's automatic mode is used to indicate that the maximum T_J has been reached. Refer to Section 5.2 for more details.
2. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
3. The storage temperature is applicable to storage conditions only. Storage within these limits will not affect the long-term reliability of the device. For functional operation, refer to the processor case temperature specifications.
4. The JEDEC, J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
5. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{SUSTAINED}$ and customer shelf life in applicable Intel box and bags.

4.6 DC Specifications

Table 4-4. Voltage and Current Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes 1,2
$V_{CC}HFM$	V_{CC} @ Highest Frequency Mode	AVID	–	1.15	V	3
$V_{CC}LFM$	V_{CC} @ Lowest Frequency Mode	0.7	–	AVID	V	3
$V_{CC}BOOT$	Default V_{CC} for initial power on		$V_{CC}LFM$		V	4
$V_{NN}BOOT$			V_{NN}		V	4
V_{NN}	V_{NN} supply voltage	0.75		0.95	V	3
V_{CCP}	V_{CCP} supply voltage	0.9975	1.05	1.1025	V	4
V_{CCQ}	V_{CCQ} supply voltage	0.9975	1.05	1.1025	V	
V_{CCPDDR}	V_{CCPDDR} supply voltage	1.029	1.05	1.071	V	5

Symbol	Parameter		Min.	Typ.	Max.	Unit	Notes [1,2]
$V_{CCPAOAC}$	$V_{CCPAOAC}$ supply voltage		0.9975	1.05	1.1025	V	
V_{MM}	V_{MM} supply voltage		1.14	1.20	1.26	V	
LVD_VBG	LVDS band gap reference voltage		1.225	1.25	1.275	V	
V_{CCA}	V_{CCA} supply voltage		1.47	1.5	1.53	V	
V_{CCA180}	V_{CCA180} supply voltage		1.746	1.8	1.854	V	
V_{CCD180}	V_{CCD180} supply voltage		1.71	1.8	1.89	V	
$V_{CC180SR}$	$V_{CC180SR}$ supply voltage		1.71	1.8	1.89	V	
V_{CC180}	V_{CC180} supply voltage		1.71	1.8	1.89	V	
I_{VCC}	Processor Number	Core Frequency	–	–	–	–	
	Z670	HFM: 1.5 GHz LFM: 0.6 GHz	–	–	2.50	A	6,7
I_{VNN}	V_{NN} supply current		–	–	1.60	A	7
I_{VCCP}	V_{CCP} supply current		–	–	0.121	A	7
I_{VCCQ}	V_{CCQ} supply current		–	–	0.015	A	7
$I_{VCCPDDR}$	V_{CCPDDR} supply current		–	–	0.150	A	7
$I_{VCCPAOAC}$	$V_{CCPAOAC}$ supply current		–	–	0.030	A	7
I_{VMM}	V_{MM} supply current		–	–	0.010	A	7
I_{VCCA}	V_{CCA} supply current		–	–	0.150	A	7
$I_{VCCA180}$	V_{CCA180} supply current		–	–	0.050	A	7,8,9
$I_{VCCD180}$	V_{CCD180} supply current		–	–		A	
$I_{VCC180SR}$	$V_{CC180SR}$ supply current		–	–	0.010	A	7
I_{VCC180}	V_{CC180} supply current		–	–	0.400	A	7

NOTES:

1. Maximum specifications are based on measurements done with currently existing workloads and test conditions. These numbers are subject to change.
2. Specified at T_J = 90°C.
3. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Note that this differs from the VID employed by the processor during a power management event (Thermal Monitor 2, Enhanced Intel SpeedStep® Technology, or Enhanced Halt State). Typical AVID range is 0.70V to 1.15V for V_{CC} and 0.75V to 0.95V for V_{NN}.
4. This specification corresponds to what value gets driven by the processor. It is possible for firmware to override these values.
5. Voltage specification of ±2% includes AC and DC variations. The sum of AC noise and DC variations should not exceed 1.05V ±2%.
6. Specified at the nominal V_{CC}.
7. Peak Sustained Current is defined as the maximum sustainable current measured as an RMS value over 1µs.

8. This is the sum of current on both rails.
9. Specification based on LVDS panel configuration of 1024x600 resolution, 60Hz refresh rate, and 18bpp color depth.

Table 4-5. Differential Clock DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Differential Clock (BCLK)						
V_{IH}	Input high voltage	–	–	1.15	V	
V_{IL}	Input low voltage	–	–	-0.3	V	
V_{CROSS}	Crossing voltage	0.3	–	0.55	V	
ΔV_{CROSS}	Range of crossing points	–	–	140	mV	
V_{SWING}	Differential output swing	300	–	–	mV	
I_{LI}	Input leakage current	-5	–	+5	µA	
C_{PAD}	Pad capacitance	1.2	1.45	2.0	pF	

Table 4-6. AGTL+, CMOS, and CMOS Open Drain Signal Group DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
GTLREF	GTL reference voltage	–	2/3 V_{CCP}	–	V	
CMREF	CMOS reference voltage	–	1/2 V_{CCP}	–	V	
R_{COMP}	Compensation resistor	27.73	27.5	27.78	Ω	10
R_{ODT}	Termination resistor	–	55	–	Ω	11
V_{IH} (GTL)	Input high voltage GTL signal	GTLREF + 0.10	V_{CCP}	V_{CCP} + 0.10	V	3, 6
V_{IL} (GTL)	Input low voltage GTL signal	-0.10	0	GTLREF – 0.10	V	2, 4
V_{IH} (CMOS)	Input high voltage CMOS signal	CMREF + 0.10	V_{CCP}	V_{CCP} + 0.10	V	3, 6
V_{IL} (CMOS)	Input low voltage CMOS signal	-0.10	0	CMREF – 0.10	V	2, 4
V_{OH}	Output high voltage	V_{CCP} – 0.10	V_{CCP}	V_{CCP}	V	6
R_{TT} (GTL)	Termination resistance	46	55	61	Ω	7
R_{TT} (CMOS)	Termination resistance	46	55	61	Ω	11
R_{ON} (GTL)	GTL buffer on resistance	21	25	29	Ω	5
R_{ON} (CMOS)	CMOS buffer on resistance	42	50	55	Ω	12
R_{ON} (CMOS_C)	CMOS common clock buffer on resistance	42	50	58	Ω	12
I_{LI}	Input leakage current	–	–	±100	µA	8
C_{PAD}	Pad capacitance	1.6	2.1	2.55	pF	9

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. VIL is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. VIH is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. VIH and VOH may experience excursions above VCCP. However, input signal drivers must comply with the signal quality specifications.
5. RON is the pull-down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at 0.33*VCCP.
6. GTLREF and CMREF should be generated from VCCP with a 1% tolerance resistor divider. The VCCP referred to in these specifications is the instantaneous VCCP.
7. RTT is the on-die termination resistance measured at VOL of the AGTL+ output driver. Measured at 0.33*VCCP. RTT is connected to VCCP on die. Refer to processor I/O buffer models for I/V characteristics.
8. Specified with on die RTT and RON are turned off. VIN between 0 and VCCP.
9. CPAD includes die capacitance only. No package parasitics are included.
10. This is the external resistor on the component pins.
11. On die termination resistance for CMOS is measured at 0.5*VCCP.
12. RON for CMOS pull-down driver resistance. Refer to processor I/O Buffer Models for I/V characteristics. Measured at 0.5*V_{CCP}.

Table 4-7. CMOS1.8 Signal Group DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{IH}	Input high voltage	(V_{CC180}/2) + 0.125	–	1.9	V	
V_{IL}	Input low voltage	-0.4	–	(V_{CC180}/2) - 0.125	V	
V_{OH}	Output high voltage	(V_{CC180}/2) + 0.25	–	–	V	
V_{OL}	Output low voltage	–	–	(V_{CC180}/2) - 0.25	V	

NOTES:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{CCP}. However, input signal drivers must comply with the signal quality specifications.

Table 4-8. LVDS Signal Group DC Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
V_{OS}	Offset voltage	1.125	1.25	1.375	V	
ΔV_{OS}	Change in offset voltage	–	–	50	mV	
V_{OD}	Differential output voltage	250	350	450	mV	

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
ΔV_{OD}	Change in differential output voltage	–	–	50	mV	
I_{SC}	Short-circuit current	–	–	12	mA	
I_{SCC}	Short-circuit comment current	–	–	24	mA	
I_L	Leakage current	-380	150	380	µA	
	Dynamic offset	–	–	150	mV	
	Overshoot	50	70	90	mV	
	Ringback	50	70	90	mV	

NOTE: Unless otherwise noted, all specifications in this table apply to all processor frequencies.

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5 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Table 4-3. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. Maintaining the proper thermal environment is the key to reliable, long-term system operation. A complete thermal solution includes both component and system level thermal management features.

Note: Trading thermal solutions also involves trading performance.

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum junction temperature (T_J) specifications at the corresponding Thermal Design Power (TDP) value listed in Table 5-1. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The maximum junction temperature is defined by an activation of the processor Intel® Thermal Monitor. Refer to Section 5.2 for more details. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 5-1. The Intel® Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section 5.2. In all cases, the Intel® Thermal Monitor feature must be enabled for the processor to remain within specification.

Table 5-1. Thermal Design Power Specifications

Symbol	Processor Number	Core Frequency	Thermal Design Power			Unit	Notes
TDP	Z670	1.5 GHz and HFM VCC 0.6 GHZ and LFM VCC	3.0			W	1,2
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**	**Notes**
Tj	Junction Temperature		0	-	90	°C	
	HD Streaming Scenario Power		-	1.02	-	W	3,4

NOTES:

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.

3. Scenario Power examines a common use case and may be more indicative of a more common power usage level as compared with the TDP. Measurement configuration assumes: LCD brightness 100nits, LCD 1024x800 10.1", USB touch panel, I^2C sensors, SDIO WiFi on, 2GB DDR2, 73% PMIC efficiency, 93% discrete VR efficiency, Flash* v10.2.
4. 720p, YouTube*.

5.1 Temperature Monitoring

The processor incorporates two methods of monitoring die temperature:

- By Intel Thermal Monitor
- By Digital Thermal Sensor (DTS)

The Intel Thermal Monitor (detailed in Section 5.2) must be used to determine when the maximum specified processor junction temperature has been reached.

5.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel® Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable.

An under- designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks or by initiating an Enhanced Intel SpeedStep® Technology transition when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There are two automatic modes called the Intel Thermal Monitor 1 (TM1) and the Intel Thermal Monitor 2 (TM2). These modes are selected by writing values to the MSRs of the processor. After the automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

The Intel® Thermal Monitor automatic mode must be enabled through IA-32 Firmware for the processor to be operating within specifications. Intel recommends that the TM1 mode and the TM2 mode be enabled on the processor.

When the TM1 mode is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50 percent duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

When the TM2 mode is enabled and a high temperature situation exists, the processor will perform an Enhanced Intel SpeedStep Technology transition to the LFM. When the processor temperature drops below the critical level, the processor will make an Enhanced Intel SpeedStep Technology transition to the last requested operating point.

The Intel Thermal Monitor automatic mode and Enhanced Intel SpeedStep Technology must be enabled through IA-32 Firmware for the processor to be operating within specifications. Intel recommends that TM1 and TM2 be enabled on the processors.

TM1 and TM2 can co-exist within the processor. If both TM1 and TM2 bits are enabled in the auto-throttle MSR, TM2 will take precedence over TM1. However, if Force TM1 over TM2 is enabled in MSRs using IA-32 Firmware and TM2 is not sufficient to cool the processor below the maximum operating temperature, then TM1 will also activate to help cool down the processor.

If a processor load-based Enhanced Intel SpeedStep Technology transition (through MSR write) is initiated when a TM2 period is active, there are two possible results:

- If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is higher than the TM2 transition based target frequency, the processor load-based transition will be deferred until the TM2 event has been completed.
- If the processor load-based Enhanced Intel SpeedStep Technology transition target frequency is lower than the TM2 transition based target frequency, the processor will transition to the processor load-based Enhanced Intel® SpeedStep® Technology target frequency point.

The TCC may also be activated using on-demand mode. If bit 4 of the ACPI Intel® Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable using bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off. However in on-demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off in 12.5% increments.

On-demand mode may be used at the same time automatic mode is enabled; however, if the system tries to enable the TCC using on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSRs, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel® Thermal Monitor feature. The Intel® Thermal Monitor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Sleep, Deep Sleep, and Deeper Sleep low power states (see Figure 3-2). If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low power states with PROCHOT# already asserted, then PROCHOT# will remain asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If the Intel Thermal Monitor automatic mode is disabled, the processor will operate out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a potentially catastrophic temperature. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

Table 5-2. Support for PROCHOT# / THERMTRIP# in Active and Idle States

System State	Core State	PROCHOT# (Bidirectional)				THERMTRIP#	
		Input		Output			
		Core	North Complex	Core	North Complex	Core	North Complex
S0	C0	Supported	Optional	Active	Active	Active	Active
	C1/C1E	Supported	Optional	Active	Active	Active	Active
	C2/C2E	Supported	Optional	Active	Active	Active	Active
	C4/C4E	Ignored	Optional	Inactive	Active	Not Guaranteed	Active
	C6	Ignored	Optional	Inactive	Active	Inactive	Active

5.2.1 Digital Thermal Sensor

The processor also contains an on die Digital Thermal Sensor (DTS) that is read using an MSR (no I/O interface). The processor has a unique digital thermal sensor that's temperature is accessible using the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation using the Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal package level low power state).

Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor (T_{J_max}). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below T_{J_max}.

Catastrophic temperature conditions are detectable using an Out of Specification status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Specification status bit is set.

The DTS-relative temperature readout corresponds to the Intel® Thermal Monitor (TM1/TM2) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 or TM2 hardware thermal control mechanism will activate. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected using two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts using the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.2.2 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 or TM2 are triggered and the temperature remains high, an "Out Of Specification" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

5.2.3 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperatures. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activity, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a potentially catastrophic processor temperature, or if the THERMTRIP# signal is asserted by the processor, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP# functionality is not ensured if the PWRGOOD signal is not asserted.

5.2.4 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 or TM2 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or deassertion of

PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals.*

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC using PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When the core's thermal sensor trips, the PROCHOT# signal is driven by the processor package. If only TM1 is enabled, PROCHOT# will be asserted and only the core that is above TCC temperature trip point will have its core clocks modulated. If TM2 is enabled and the core is above TCC temperature trip point, it will enter the lowest programmed TM2 performance state. It is important to note that Intel recommends that both TM1 and TM2 be enabled.

When PROCHOT# is driven by an external agent, if only TM1 is enabled on the core, then the processor core will have the clocks modulated. If TM2 is enabled, then the processor core will enter the lowest programmed TM2 performance state. It should be noted that Force TM1 on TM2, enabled using IA-32 Firmware, does not have any effect on external PROCHOT#. If PROCHOT# is driven by an external agent when TM1, TM2, and Force TM1 on TM2 are all enabled, then the processor will still apply only TM2.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption.

Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power-intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

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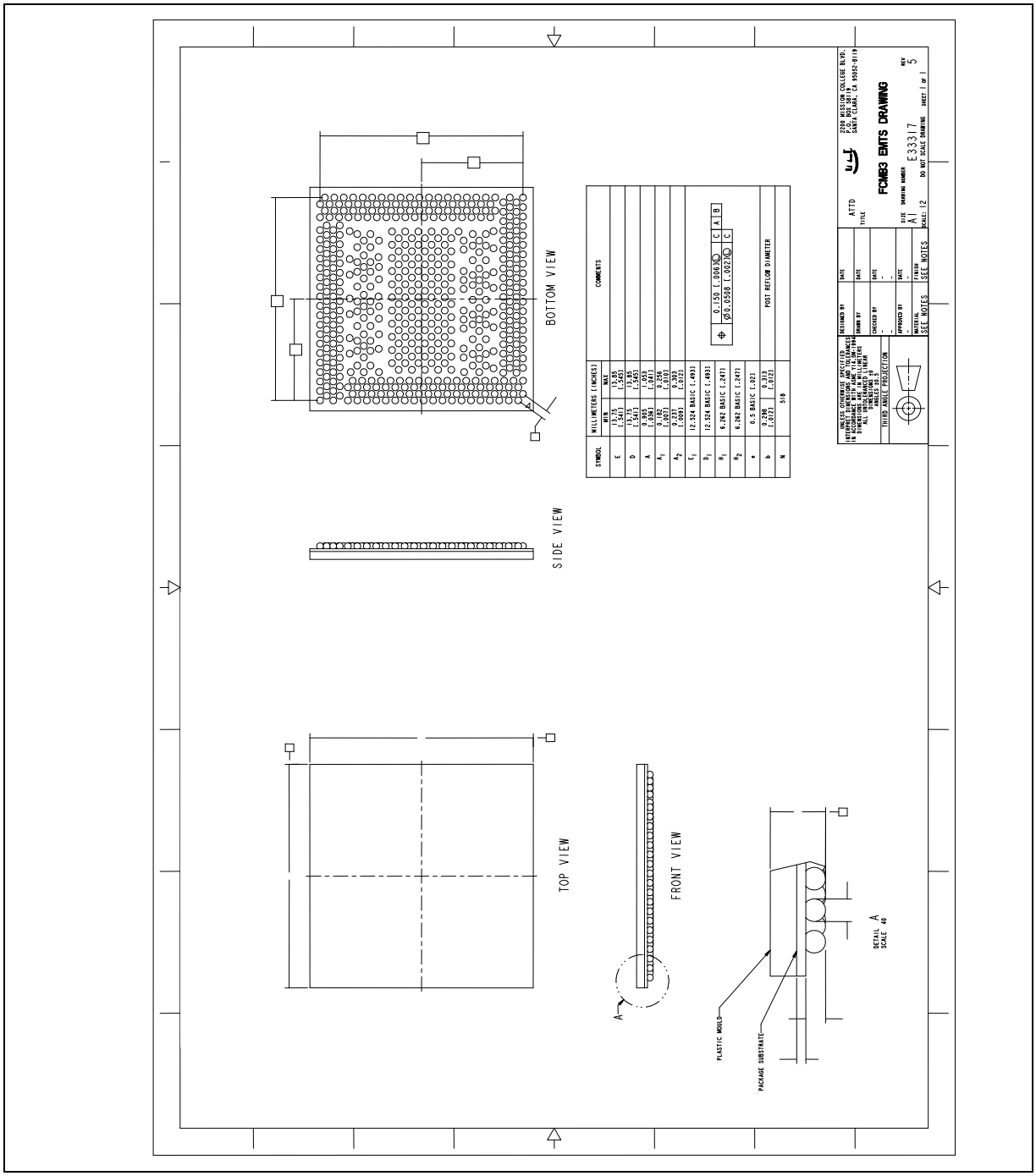
6 Package Mechanical Specifications and Pin Information

This chapter describes the package specifications and pinout assignments.

6.1 Package Mechanical Specifications

The processor will be available in a 518 pin FCMB3 package. The package dimensions are shown in Figure 6-1.

Figure 6-1. Package Mechanical Drawing



6.2 Processor Pinout Assignment

Table 6-1, Table 6-2 and Table 6-3 are graphic representations of the processor pinout assignments. Table 6-4 lists the pinout by signal name.

Table 6-1. Processor Pinout (Top View—Columns 21–31)

	31	30	29	28	27	26	25	24	23	22	21	
AL	V_{SS}	V_{SS}	CDVO_TX3	CDVO_TX2	CDVO_TXSTB_ODD#		CDVO_CVREF	CDMI_RXCHAR#		CDMI_RXSTB_EVEN#	CDMI_RX6	AL
AK		CDVO_TXDPWR#		CDVO_TX4	CDVO_TX0	CDVO_TXSTB_EVEN#		CDVO_RCOMP0	CDVO_VBLANK#	CDMI_RXSTB_ODD#		AK
AJ	LA_DATAP0	LA_DATAN0	V_{SS}	LA_DATAP1	V_{SS}		V_{SS}	V_{SS}		V_{SS}	V_{SS}	AJ
AH	LA_CLKP		V_{SS}		CDVO_STALL#	CDVO_TX5		CDVO_TX1	CDVO_RCOMP1	V_{CCQ_2}		AH
AG		LA_CLKN		LA_DATAN1		V_{SS}				V_{SS}		AG
AF	LA_DATAN2	LA_DATAP2	V_{SS}	LA_DATAN3		V_{CCD180}		V_{CCA180}		V_{CCP}		AF
AE	LA_IBG		V_{SS}				V_{SS}		V_{SS}		V_{SS}	AE
AD	RSVD	LA_VBG	V_{SS}	LA_DATAP3		V_{CCD180}		V_{CCA180}		V_{CCP}		AD
AC		RSVD		V_{CCP}			V_{SS}			V_{SS}	V_{SS}	AC
AB	TP3		V_{SS}									AB
AA	TP5	TP4	V_{SS}	$V_{CCPAOAC}$		V_{NN}		RSVD9		V_{CC}		AA
Y		TP6		RSVD8			V_{NN}		V_{SS}		V_{SS}	Y
W	TP2	TP1	V_{SS}	THRMDA		V_{NN}		V_{CC}		V_{CC}		W
V	TP7		V_{SS}				V_{NN}		V_{SS}		V_{SS}	V
U		TP8		THRMDC		V_{NN}		V_{CC}		V_{CC}		U
T	TP9	TP10	VNNSENSE	V_{SS}			V_{NN}		V_{SS}		V_{SS}	T
R	V_{NN}		V_{NN}			V_{NN}		V_{NN}		V_{NN}		R
P	V_{SS}	V_{NN}	V_{SS}	V_{NN}			V_{NN}		V_{SS}		V_{SS}	P
N		V_{NN}		V_{NN}		V_{NN}		V_{NN}		V_{NN}		N
M	V_{NN}	V_{CC180}	V_{NN}	V_{CC180}			V_{NN}		V_{SS}		V_{SS}	M
L	V_{CC180}		V_{CC180}			V_{NN}						L
K		V_{CC180}		V_{CC180}			V_{SS}	V_{SS}				K
J	SM_DQ1	SM_DQ0	V_{SS}	SM_BS2								J
H	SM_DQ3		V_{SS}			V_{CC180}		V_{CC180}		V_{CCPDDR}		H
G	SM_DQS1	SM_DQ2	V_{SS}	SM_BS1			V_{SS}		V_{SS}		V_{SS}	G
F		SM_DM0		SM_MA2		V_{CC180}		V_{CC180}		V_{CCPDDR}		F
E	SM_DQ5		V_{SS}			V_{SS}		V_{SS}				E
D	SSM_DQ4		SM_MA4	SM_MA12		SM_BS0	SM_MA3	SM_MA7		SM_MA8	SM_MA0	D
C	SM_DQ6	V_{SS}	VSS		V_{SS}	V_{SS}		V_{SS}	V_{SS}		V_{SS}	C
B	SM_DQ7		SM_DQ8	SM_DQ10		SM_DQS0	SM_DQ12	SM_DQ14		SM_RCVENOUT	SM_RCVENIN	B
A	V_{SS}	SM_DQ9	SM_DQ11		SM_DM1	SM_MA10		SM_DQ13	SM_DQ15		SM_MA1	A
	31	30	29	28	27	26	25	24	23	22	21	

Table 6-2. Processor Pinout (Top View—Columns 11–20)

	20	19	18	17	16	15	14	13	12	11	
AL		CDMI_RX4	CDMI_RX1	CDMI_CVREF		CDMI_TXDPWR#	CDMI_TX6		CDMI_TX3	CDMI_TX1	AL
AK	CDMI_RX7	CDMI_RX3		CDMI_RX0	CDMI_GVREF		CDMI_TX7	CDMI_TX4	CDMI_TX2		AK
AJ		V_{SS}	V_{SS}	V_{SS}		V_{SS}	V_{SS}		V_{SS}	V_{SS}	AJ
AH	CDMI_RXDPWR#	CDMI_RX5		CDMI_RX2	CDMI_TXCHAR#		CDMI_TX5	CDMI_TX0	V_{CCQ_1}		AH
AG	V_{SS}				V_{SS}		V_{SS}				AG
AF	CDVO_GVREF		V_{NN}		V_{CCP}		V_{CCP}		V_{NN}		AF
AE		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	AE
AD	V_{CCP}		V_{NN}		V_{CCP}		V_{CCP}		V_{NN}		AD
AC		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	AC
AB											AB
AA	V_{CC}		V_{CC}		V_{CC}		V_{CC}		V_{CC}		AA
Y		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	Y
W	V_{CC}		V_{CC}		V_{CC}		V_{CC}		V_{CC}		W
V		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	V
U	V_{CC}		V_{CC}		V_{CC}		V_{CC}		V_{CC}		U
T		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	T
R	V_{NN}		V_{NN}		V_{NN}		V_{NN}		V_{NN}		R
P		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	P
N	V_{NN}		V_{NN}		V_{NN}		V_{NN}		V_{NN}		N
M		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	M
L											L
K	V_{SS}	V_{SS}	V_{SS}				V_{SS}	V_{SS}	V_{SS}		K
J											J
H	V_{CC180}		V_{CC180}		V_{CCPDDR}		V_{CC180}		V_{CC180}		H
G		V_{SS}		V_{SS}		V_{SS}		V_{SS}		V_{SS}	G
F	V_{CC180}		V_{CC180}		V_{CCPDDR}		V_{CC180}		V_{CC180}		F
E	V_{SS}		V_{SS}				V_{SS}		V_{SS}		E
D		SM_CK0	SM_CK0#		$V_{CC180SR}$	RSVD	SM_MA14		SM_RAS#	SM_WE#	D
C	V_{SS}	V_{SS}		V_{SS}	V_{SS}		V_{SS}	V_{SS}	V_{SS}		C
B		SM_RCOMP	SM_MA6		SM_SREN#	SM_MA11	SM_DQ25		SM_DQ27	SM_DQS3	B
A	SM_MA9	SM_CKE0		SM_CKE1	SM_MA5		SM_MA13	SM_DQ24	SM_DQ26		A
	20	19	18	17	16	15	14	13	12	11	

Table 6-3. Processor Pinout (Top View—Columns 1–10)

	10	9	8	7	6	5	4	3	2	1	
AL		CDMI_TXSTB_ODD#	CDMI_RCOMP1	PRDY#		BPM2#	BPM1#		VID6	V_{SS}	AL
AK	CDMI_TXSTB_EVEN#	CDMI_RCOMP0		GTLREF0	PREQ#		BPM3#	RSVD	VID4		AK
AJ		V_{SS}	V_{SS}	V_{SS}		V_{SS}	V_{SS}		V_{SS}	VID1	AJ
AH	IERR	BPM0#		RSVD	VID5		VID2	VID3	VID0		AH
AG	V_{SS}		V_{SS}			V_{SS}	RSVD	V_{SS}	RSVD	RSVD	AG
AF	V_{CCP}		V_{CCP}		V_{NN}			V_{SS}		PROCHOT#	AF
AE		V_{SS}		V_{SS}		V_{SS}	THERMTRIP#		PWRMODE1		AE
AD	V_{CCP}		V_{CCP}		V_{NN}		VIDEN0	V_{SS}	PWRMODE2	VIDEN1	AD
AC		V_{SS}				V_{CCP}		V_{SS}		PWRMODE0	AC
AB							$V_{CCPAOAC}$	V_{CC}	V_{SS}	V_{CC}	AB
AA	V_{CC}		V_{CC}	V_{CC}			V_{CC}		V_{CC}		AA
Y		V_{SS}	V_{SS}		V_{SS}			V_{SS}		V_{SS}	Y
W	V_{CC}		V_{CC}	V_{CC}			V_{CC}	V_{CC}	V_{CC}	V_{CC}	W
V		V_{SS}	V_{SS}		VSSSENSE		V_{SS}		V_{SS}		V
U	V_{CC}		V_{CC}	V_{CC}			V_{CC}	V_{CC}	V_{CC}	V_{CC}	U
T		V_{SS}	V_{SS}		V_{CCA}			VCCSENSE		V_{CCA}	T
R	V_{NN}		V_{NN}	V_{NN}			V_{SS}		V_{SS}		R
P		V_{SS}	V_{SS}		V_{CCA}		RSVD	V_{SS}	RSVD	$V_{CCPAOAC}$	P
N	V_{NN}		V_{NN}	V_{SS}				V_{SS}		BCLK_N	N
M		V_{SS}	V_{SS}		V_{CCP}		RSVD	V_{SS}	BCLK_P	RSVD	M
L							RSVD		RSVD		L
K		V_{SS}		V_{CCP}		$V_{CCPAOAC}$		V_{SS}		RSVD	K
J							V_{SS}	V_{SS}	TMS	TRST#	J
H	V_{CCPDDR}		V_{CC180}		V_{CCP}		TDO		TCK		H
G		V_{SS}		V_{SS}		V_{SS}	BSEL1	V_{SS}	RSVD	V_{SS}	G
F	V_{CCPDDR}		V_{CC180}		V_{CCP}			V_{SS}		TDI	F
E			V_{SS}		V_{SS}		SM_CAS#		RSVD		E
D		SM_ODT0	SM_ODT1	SM_CS1#		SM_CS0#	GTLREF1	V_{SS}	SM_DQ23	SM_DQ22	D
C	V_{SS}	V_{SS}		V_{SS}	V_{SS}			V_{SS}		SM_DQ20	C
B		SM_DQ29	SM_DQ31	SM_DQ17		SM_DQ19	SM_DM2	SM_DQS2	SM_DQ21	V_{SS}	B
A	SM_DM3	SM_DQ28		SM_DQ30	SM_DQ16		SM_DQ18		V_{SS}		A
	10	9	8	7	6	5	4	3	2	1	

Table 6-4. Pinout—Ordered by Signal Name

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
BCLK_P	M2	CDMI_TXSTB_EVEN#	AK10	TP6	Y30
BCLK_N	N1	CDVO_CVREF	AL25	TP8	U30
BPM0#	AH9	CDVO_TXDPWR#	AK30	TP10	T30
BPM1#	AL4	CDVO_GVREF	AF20	TP3	AB31
BPM2#	AL5	CDVO_RCOMP0	AK24	TP5	AA31
BPM3#	AK4	CDVO_RCOMP1	AH23	TP7	V31
BSEL1	G4	CDVO_STALL#	AH27	TP9	T31
CDMI_CVREF	AL17	CDVO_TX0	AK27	RSVD8	Y28
CDMI_RXDPWR#	AH20	CDVO_TX1	AH24	PRDY#	AL7
CDMI_TXDPWR#	AL15	CDVO_TX2	AL28	PREQ#	AK6
CDMI_GVREF	AK16	CDVO_TX3	AL29	PROCHOT#	AF1
CDMI_RCOMP0	AK9	CDVO_TX4	AK28	PWRMODE0	AC1
CDMI_RCOMP1	AL8	CDVO_TX5	AH26	PWRMODE1	AE2
CDMI_RX0	AK17	CDVO_TXSTB_ODD#	AL27	PWRMODE2	AD2
CDMI_RX1	AL18	CDVO_TXSTB_EVEN#	AK26	SM_ODT1	D8
CDMI_RX2	AH17	CDVO_VBLANK#	AK23	SM_ODT0	D9
CDMI_RX3	AK19	GTLREF0	AK7	RSVD7	E2
CDMI_RX4	AL19	GTLREF1	D4	SM_BS0	D26
CDMI_RX5	AH19	IERR	AH10	SM_BS1	G28
CDMI_RX6	AL21	LA_CLKN	AG30	SM_BS2	J28
CDMI_RX7	AK20	LA_CLKP	AH31	SM_CAS#	E4
CDMI_RXCHAR#	AL24	LA_DATAN0	AJ30	SM_CK0	D19
CDMI_RXSTB_ODD#	AK22	LA_DATAN1	AG28	SM_CK0#	D18
CDMI_RXSTB_EVEN#	AL22	LA_DATAN2	AF31	SM_CKE0	A19
CDMI_TX0	AH13	LA_DATAN3	AF28	SM_CKE1	A17
CDMI_TX1	AL11	LA_DATAP0	AJ31	SM_CS0#	D5
CDMI_TX2	AK12	LA_DATAP1	AJ28	SM_CS1#	D7
CDMI_TX3	AL12	LA_DATAP2	AF30	SM_DM0	F30
CDMI_TX4	AK13	LA_DATAP3	AD28	SM_DM1	A27
CDMI_TX5	AH14	LA_IBG	AE31	SM_DM2	B4
CDMI_TX6	AL14	LA_VBG	AD30	SM_DM3	A10
CDMI_TX7	AK14	TP1	W30	SM_DQ0	J30
CDMI_TXCHAR#	AH16	TP2	W31	SM_DQ1	J31
CDMI_TXSTB_ODD#	AL9	TP4	AA30	SM_DQ10	B28

Pin Name	Pin #
SM_DQ11	A29
SM_DQ12	B25
SM_DQ13	A24
SM_DQ14	B24
SM_DQ15	A23
SM_DQ16	A6
SM_DQ17	B7
SM_DQ18	A4
SM_DQ19	B5
SM_DQ2	G30
SM_DQ20	C1
SM_DQ21	B2
SM_DQ22	D1
SM_DQ23	D2
SM_DQ24	A13
SM_DQ25	B14
SM_DQ26	A12
SM_DQ27	B12
SM_DQ28	A9
SM_DQ29	B9
SM_DQ3	H31
SM_DQ30	A7
SM_DQ31	B8
SM_DQ4	D31
SM_DQ5	E31
SM_DQ6	C31
SM_DQ7	B31
SM_DQ8	B29
SM_DQ9	A30
SM_DQS0	B26
SM_DQS1	G31
SM_DQS2	B3
SM_DQS3	B11
SM_MA0	D21
SM_MA1	A21

Pin Name	Pin #
SM_MA2	F28
SM_MA3	D25
SM_MA4	D29
SM_MA5	A16
SM_MA6	B18
SM_MA7	D24
SM_MA8	D22
SM_MA9	A20
SM_MA10	A26
SM_MA11	B15
SM_MA12	D28
SM_MA13	A14
SM_MA14	D14
SM_RAS#	D12
SM_RCOMP	B19
SM_RCVENIN	B21
SM_RCVENOUT	B22
SM_SREN#	B16
SM_WE#	D11
TCK	H2
TDI	F1
TDO	H4
RSVD	D15
RSVD	G2
RSVD	L2
RSVD	L4
RSVD	K1
RSVD	M4
RSVD	M1
RSVD	P2
RSVD	P4
RSVD	U28
RSVD	W28
RSVD	AK3
RSVD	AG1

Pin Name	Pin #
RSVD	AG2
RSVD	AG4
RSVD	AH7
THERMTRIP#	AE4
TMS	J2
TRST#	J1
VCC	AA10
VCC	AA12
VCC	AA14
VCC	AA16
VCC	AA18
VCC	AA2
VCC	AA20
VCC	AA22
VCC	AA4
VCC	AA7
VCC	AA8
VCC	AB1
VCC	AB3
VCC	U1
VCC	U10
VCC	U12
VCC	U14
VCC	U16
VCC	U18
VCC	U2
VCC	U20
VCC	U22
VCC	U24
VCC	U3
VCC	U4
VCC	U7
VCC	U8
VCC	W1
VCC	W10

Pin Name	Pin #
VCC	W12
VCC	W14
VCC	W16
VCC	W18
VCC	W2
VCC	W20
VCC	W22
VCC	W24
VCC	W3
VCC	W4
VCC	W7
VCC	W8
VCC180	F12
VCC180	F14
VCC180	F18
VCC180	F20
VCC180	F24
VCC180	F26
VCC180	F8
VCC180	H12
VCC180	H14
VCC180	H18
VCC180	H20
VCC180	H24
VCC180	H26
VCC180	H8
VCC180	K28
VCC180	K30
VCC180	L29
VCC180	L31
VCC180	M28
VCC180	M30
VCC180SR	D16
VCCA	P6
VCCA	T1

Pin Name	Pin #
VCCA	T6
VCCA180	AD24
VCCA180	AF24
VCCD180	AD26
VCCD180	AF26
VCCP	K7
VCCP	AC28
VCCP	AC5
VCCP	AD10
VCCP	AD14
VCCP	AD16
VCCP	AD20
VCCP	AD22
VCCP	AD8
VCCP	AF10
VCCP	AF14
VCCP	AF16
VCCP	AF22
VCCP	AF8
VCCP	F6
VCCP	H6
VCCP	M6
VCCQ_1	AH12
VCCQ_2	AH22
VCCPAOAC	AB4
VCCPAOAC	AA28
VCCPAOAC	K5
VCCPAOAC	P1
VCCPDDR	F10
VCCPDDR	F16
VCCPDDR	F22
VCCPDDR	H10
VCCPDDR	H16
VCCPDDR	H22
VCCSENSE	T3

Pin Name	Pin #
VID0	AH2
VID1	AJ1
VID2	AH4
VID3	AH3
VID4	AK2
VID5	AH6
VID6	AL2
VIDEN0	AD4
VIDEN1	AD1
RSVD9	AA24
VNN	AA26
VNN	AD12
VNN	AD18
VNN	AD6
VNN	AF12
VNN	AF18
VNN	AF6
VNN	L26
VNN	M25
VNN	M29
VNN	M31
VNN	N10
VNN	N12
VNN	N14
VNN	N16
VNN	N18
VNN	N20
VNN	N22
VNN	N24
VNN	N26
VNN	N28
VNN	N30
VNN	N8
VNN	P25
VNN	P28

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
VNN	P30	VSS	AC30	VSS	AJ2
VNN	R10	VSS	AD29	VSS	AJ21
VNN	R12	VSS	AD3	VSS	AJ22
VNN	R14	VSS	AD31	VSS	AJ24
VNN	R16	VSS	AE11	VSS	AJ25
VNN	R18	VSS	AE13	VSS	AJ27
VNN	R20	VSS	AE15	VSS	AJ29
VNN	R22	VSS	AE17	VSS	AJ4
VNN	R24	VSS	AE19	VSS	AJ5
VNN	R26	VSS	AE21	VSS	AJ7
VNN	R29	VSS	AE23	VSS	AJ8
VNN	R31	VSS	AE25	VSS	AJ9
VNN	R7	VSS	AE29	VSS	AL1
VNN	R8	VSS	AE5	VSS	AL30
VNN	T25	VSS	AE7	VSS	AL31
VNN	U26	VSS	AE9	VSS	B1
VNN	V25	VSS	AF29	VSS	C10
VNN	W26	VSS	AF3	VSS	C12
VNN	Y25	VSS	AG10	VSS	C13
VNNSENSE	T29	VSS	AG14	VSS	C14
VSS	A2	VSS	AG16	VSS	C16
VSS	A31	VSS	AG20	VSS	C17
VSS	AA29	VSS	AG22	VSS	C19
VSS	AB2	VSS	AG26	VSS	C20
VSS	AB29	VSS	AG3	VSS	C21
VSS	AC11	VSS	AG5	VSS	C23
VSS	AC13	VSS	AG8	VSS	C24
VSS	AC15	VSS	AH29	VSS	C26
VSS	AC17	VSS	AJ11	VSS	C27
VSS	AC19	VSS	AJ12	VSS	C29
VSS	AC21	VSS	AJ14	VSS	C3
VSS	AC22	VSS	AJ15	VSS	C30
VSS	AC25	VSS	AJ17	VSS	C6
VSS	AC3	VSS	AJ18	VSS	C7
VSS	AC9	VSS	AJ19	VSS	C9

Pin Name	Pin #
VSS	D3
VSS	E12
VSS	E14
VSS	E18
VSS	E20
VSS	E24
VSS	E26
VSS	E29
VSS	E6
VSS	E8
VSS	F3
VSS	G11
VSS	G13
VSS	G15
VSS	G17
VSS	G19
VSS	G21
VSS	G23
VSS	G25
VSS	G29
VSS	G3
VSS	G5
VSS	G7
VSS	G9
VSS	H29
VSS	J29
VSS	J3
VSS	J4
VSS	K12
VSS	K13
VSS	K14
VSS	K18
VSS	K19
VSS	K20
VSS	K24

Pin Name	Pin #
VSS	K25
VSS	K3
VSS	K9
VSS	M11
VSS	M13
VSS	M15
VSS	M17
VSS	M19
VSS	M21
VSS	M23
VSS	M3
VSS	M8
VSS	M9
VSS	N3
VSS	N7
VSS	P11
VSS	P13
VSS	P15
VSS	P17
VSS	P19
VSS	P21
VSS	P23
VSS	P29
VSS	P3
VSS	P31
VSS	P8
VSS	P9
VSS	R2
VSS	R4
VSS	T11
VSS	T13
VSS	T15
VSS	T17
VSS	T19
VSS	T21

Pin Name	Pin #
VSS	T23
VSS	T28
VSS	T8
VSS	T9
VSS	V11
VSS	V13
VSS	V15
VSS	V17
VSS	V19
VSS	V2
VSS	V21
VSS	V23
VSS	V29
VSS	V4
VSS	V8
VSS	V9
VSS	W29
VSS	Y1
VSS	Y11
VSS	Y13
VSS	Y15
VSS	Y17
VSS	Y19
VSS	Y21
VSS	Y23
VSS	Y3
VSS	Y6
VSS	Y8
VSS	Y9
VSS	G1
VSSSENSE	V6

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